



Att'y. Docket No.: 3175-Z

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Je 7/31/06

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Laung-Terng Wang et al

Serial No. 10/086,214

Examiner James C. Kerveros

Filed: March 27, 2002

Art Unit 2133

For: Method and Apparatus for Diagnosing Failures in an Integrated  
Circuit Using Design-for-Debug (DFD) Techniques

**AMENDMENT AFTER FINAL**

MAIL STOP AF  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

In response to the Office Action mailed October 5, 2005,  
applicants respond as follows: